AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A semiconductor processing system comprising an interface control circuit and a processing circuit, and attached to an external apparatus so as to receive an operation power supply therefrom,

wherein said interface control circuit, when said system is removed from the external apparatus, detects a potential change that occurs at a first external terminal of said system which is disconnected from a predetermined terminal of the external apparatus before the power supply from the external apparatus is disconnected from a second external terminal of said system, then instructs the processing circuit that is active to perform an ending processing, and

wherein the first external terminal is one of a plurality of ground terminals and said first external terminal is connected to a power supply terminal through a resistance element.

2. (currently amended) A semiconductor processing system comprising an interface control circuit and a processing circuit, and attached to an external apparatus so as to receive an operation power supply therefrom,

wherein said interface control circuit, when said system is removed from the external apparatus, detects a potential change that occurs at a first external terminal of said system which is disconnected from a predetermined terminal of the external apparatus before the power supply from said external apparatus is disconnected from a second external terminal of said system, then stores a flag denoting an occurrence of the power supply shutoff,

wherein said first external terminal is a reset terminal to be set at a first voltage after a reset instruction is completed, and

wherein said reset terminal is coupled to the second external terminal provided in the semiconductor processing system through a resistance element while said second external terminal receives a second voltage from the external apparatus, the polarity of said second voltage being opposite from that of said first voltage.

3. (currently amended) A semiconductor processing system comprising an interface control circuit and a

processing circuit and attached to an external apparatus so as to receive an operation power supply therefrom,

wherein said interface control circuit, when said system is removed from the external apparatus, detects a potential change that occurs at a first external terminal of said system which is disconnected from a predetermined terminal of the external apparatus before the power supply from the external apparatus is disconnected from a second external terminal of said system, then starts up a power supply circuit to supplement the operation power supply of the processing circuit,

wherein said first external terminal receives a first voltage when the processing circuit is active and said first external terminal is coupled to said second external terminal provided in the semiconductor processing system through a resistance element, and

wherein said second external terminal receives a second voltage from the external apparatus, the polarity of said second voltage being opposite from that of said first voltage.

4. (previously presented) The semiconductor processing system according to claim 1,

wherein said system includes a monitoring terminal coupled to said first external terminal, and

wherein the monitoring terminal enables the external apparatus to monitor said potential change that occurs at said first external terminal after said first external terminal is disconnected from the external apparatus.

5-6. (cancelled)

7. (currently amended) The semiconductor processing system according to claim ~~5~~2,

wherein said first voltage is a ground voltage and said second voltage is a supply voltage while said second external terminal is an external power supply terminal.

8. (currently amended) The semiconductor processing system according to claim ~~6~~3,

wherein said first voltage is a supply voltage and said second voltage is a circuit ground voltage while said second external terminal is a ground source terminal.

9. (cancelled)

10. (original) The semiconductor processing system according to claim 1,

wherein said processing circuit includes a non-volatile memory enabling information to be written/erased therein/therefrom electrically; and

wherein said interface control circuit is a control circuit for controlling both of said external interface and said non-volatile memory.

11. (original) The semiconductor processing system according to claim 10,

wherein said ending processing adjusts threshold voltages of non-volatile memory cells so as to be set in a predetermined threshold voltage range during an erasure/write processing.

12. (original) The semiconductor processing system according to claim 10,

wherein said ending processing sets and stores an identification flag that can identify a block of non-volatile memory cells during an erasure/write processing.

13. (original) The semiconductor processing system according to claim 12,

wherein said ending processing includes a completing processing for the current erasure/write processing for a non-volatile memory cell.

14. (previously presented) A semiconductor processing system, comprising:

a plurality of external terminals, each of which is attachable/detachable to/from its corresponding terminal of an external apparatus;

a first processing circuit coupled to said plurality of external terminals;

a second processing circuit controlled by said first processing circuit; and

a resistance element used for connection between a first external terminal and a second external terminal among said plurality of external terminals,

wherein said first external terminal receives a first voltage when said second processing circuit is active,

wherein said second external terminal receives a second voltage, and

wherein said first processing circuit, when the system is removed from said external apparatus, detects a voltage change from said first voltage to said second voltage at said first external terminal before power supply from the

external apparatus is disconnected from said second external terminal, then executes a processing in response to the detected voltage change.

15. (original) The semiconductor processing system according to claim 14,

wherein said first external terminal is a reset terminal that receives a first voltage after a reset instruction is completed.

16. (previously presented) A semiconductor processing system, comprising:

a plurality of external terminals, each of which is attachable/detachable to/from its corresponding terminal of an external apparatus;

a first processing circuit coupled to said plurality of external terminals;

a second processing circuit controlled by said first processing circuit; and

a resistance element used for connection between a first external terminal and a second external terminal among said plurality of external terminals,

wherein said first external terminal is one of a plurality of ground terminals,

wherein said second external terminal is a power supply terminal, and .

wherein said first processing circuit, when the system is removed from said external apparatus, detects a voltage change from a ground voltage to a supply voltage thereof at said first external terminal before power supply from the external apparatus is disconnected from said second external terminal, then executes a processing in response to the detected voltage change.

17. (original) The semiconductor processing system according to claim 16,

wherein said first external terminal is disposed so as to be disconnected from its corresponding terminal of said external apparatus earlier than other ground terminals when the system is removed from said external apparatus.

18. (original) The semiconductor processing system according to claim 16,

wherein said second processing circuit includes a non-volatile memory enabling information to be written/erased therein/therefrom electrically, and

wherein said first processing circuit is a control circuit for controlling both of said external interface and said non-volatile memory.

19. (previously presented) The semiconductor processing system according to claim 1, wherein said first and second external terminals have different lengths.

20. (previously presented) The semiconductor processing system according to claim 2, wherein said first and second external terminals have different lengths.

21. (previously presented) The semiconductor processing system according to claim 3, wherein said first and second external terminals have different lengths.

22. (previously presented) The semiconductor processing system according to claim 14, wherein said plurality of external terminals includes external terminals having different lengths.

23. (previously presented) The semiconductor processing system according to claim 16, wherein said plurality of

external terminals includes external terminals having different lengths.